NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

INTEL CORPORATION,
Appellant

v.

PACT XPP SCHWEIZ AG,
Appellee

2022-1038

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2020-00531.

Decided: February 24, 2023

NATHAN S. MAMMEN, Kirkland & Ellis LLP, Washington, DC, argued for appellant. Also represented by DIVA R. HOLLIS, JOHN C. O'QUINN; ROBERT ALAN APPLEBY, New York, NY.

SANFORD IAN WEISBURST, Quinn Emanuel Urquhart & Sullivan, LLP, New York, NY, argued for appellee. Also represented by NIMA HEFAZI, FREDERICK A. LORIG, Los Angeles, CA; MARK YEH-KAI TUNG, Redwood Shores, CA.

Before NEWMAN, PROST, and HUGHES, *Circuit Judges*.

Hughes, *Circuit Judge*.

PACT XPP Schweiz AG owns U.S. Patent No. 9,436,631, which discloses and claims reconfigurable bus systems for transferring data between components of multiprocessor systems. On a petition for inter partes review filed by Intel Corp., the Patent and Trademark Office's Patent Trial and Appeal Board instituted review and found claim 4 to be nonobvious. We reverse.

I

This case is about "bus systems," which are systems that transfer data between components inside a computer. The '631 patent discloses a "[r]econfigurable architecture" including "modules . . . which are interconnected directly or via a bus system." '631 patent at 1:40–46. The patent describes the architecture as comprising "Processing Array Elements," which are simply the processing components (e.g., processors or memory) in the '631 patent's reconfigurable architecture. '631 patent at 2:3–9.

Claims 1–4 are relevant to this appeal. Claim 1 reads:

> 1. A bus system for transferring data between parts of a multiprocessor system, the bus system comprising:
>
> > a plurality of bus segments for each processor of the multiprocessor system comprising a plurality of flexible data channels to each processor of the multiprocessor system according to algorithms to be executed, wherein a plurality of algorithms may executed in parallel;
> >
> > wherein a communication between a sender and a receiver is established in accordance with a data transfer for an executed algorithm; and

> at least one identifier is transmitted with the data for at least one of: identifying a source of the data transfer; and selecting a target of the data transfer.

'631 patent at 34:20–33. Claim 2 depends from claim 1, and adds "wherein at least one of the parts of the multiprocessor system is a cache memory." '631 patent at 34:34–35. Claim 3 depends from claim 2 and adds "wherein the cache memory comprises a plurality of cache cores." '631 patent at 34:36–37. Claim 4, the claim at issue on appeal, depends from claim 3 and reads:

> 4. The bus system of claim 3, wherein the cache cores are connected to the bus system such that for the data transfer one of the cache cores is selected according to an address transferred via the bus system; *wherein at least some of the plurality of cache cores are combined to form a large cache*.

'631 patent at 34:38–43 (emphasis added).

Intel petitioned for inter partes review of claims 1–4 of the '631 patent. Relevant to our decision, the petition asserts that claim 1 is obvious under U.S. Patent No. 5,761,455 (King) and that claims 2–4 are obvious under King in combination with U.S. Patent No. 5,893,163 (Arimilli).

King teaches that "the bottleneck which limits processing speed is the interface between the processor and memory." King at 1:37–39. The bus system disclosed by King tries to solve this bottleneck through "coupling processors and memories efficiently . . . to allow processors in a multi-processor system to access memories with a minimum of contention and a maximum use of the available ports to the memories." King at 1:46–50. It is undisputed that King's bus system meets every limitation of claim 1. And while King's bus system does not use caches to improve the processing speed, King does teach that "on-chip

memory caching" is another method for reducing the bottleneck. King at 1:39–40.

Arimilli, like King, is directed to improving multiprocessor systems. Arimilli teaches that the "latency associated with accessing system memory [is] quite large" compared to the latency associated with accessing cache memory. Arimilli at 1:60–64. Consequently, Arimilli's solution for reducing latency is "maintain[ing] as much useful data in at least one of the cache memories as possible[.]" *Id.* Arimilli accomplishes this goal by disclosing multiprocessor systems using three levels of caches: primary L1, secondary L2, and tertiary L3. Each processing unit's L3 cache can operate in a "shared" mode, wherein all "L3 caches . . . are combined" to represent "different segments that "[make] up the entire address spaces of the system memory." Arimilli at 4:64–5:3.

After Intel filed the petition and before filing its preliminary response, PACT statutorily disclaimed claims 1–3 of the '631 patent. The Board then instituted inter partes review on claim 4.

Although the only remaining challenged claim was claim 4, the Board's final written decision also addressed the validity of disclaimed claims 1–3 "since claim 4 depends, successively, from each of these other claims." *Intel Corp. v. PACT XPP Schweiz AG*, IPR2020-00531, Paper 37 at 7 (P.T.A.B. Aug. 10, 2021) (*Board Decision*). The Board found "that King discloses each limitation of claim 1[.]" *Board Decision* at 30. For claims 2 and 3—which add the requirements that the system includes cache memory and that the cache memory comprises a plurality of cache cores—the Board again agreed with Intel that the combination of King and Arimilli teaches all the limitations of claims 2 and 3 and that there was "a persuasive rationale" why an artisan of ordinary skill would have incorporated Arimilli's L1 and L2 caches into King's system to achieve the claimed bus system. *Board Decision* at 30–33.

For claim 4, which requires that cache cores are connected to the bus system and that at least some of the cache cores are combined to form a large cache, the Board found that Intel had not met its burden to show that claim was obvious. The Board found that Intel, who had argued that Arimilli's L3 caches operating in shared mode taught claim 4's additional limitation, had not established a motivation to combine because "Intel has not specifically explained how a person of ordinary skill in the art would have modified King[] . . . to incorporate a shared bus as disclosed in Arimilli." *Board Decision* at 38.

Intel appeals the Board's conclusion that claim 4 of the '631 patent is nonobvious under King and Arimilli.[1] We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

II

A

"Whether a claimed invention would have been obvious is a question of law, based on factual determinations regarding the scope and content of the prior art, differences between the prior art and claims at issue, the level of ordinary skill in the pertinent art, [and] the motivations to modify or combine prior art . . . ." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). We review the Board's legal determinations de novo and its underlying factual determinations for substantial evidence. *Rambus Inc. v. Rea*, 731 F.3d 1248, 1251 (Fed. Cir. 2013). Substantial evidence "means such relevant evidence as a

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[1] Intel's petition also included another obviousness ground for claim 4 that the Board rejected in its final written decision. Intel argues that the Board's rejection of this other ground was also in error. Because our resolution of the ground concerning King and Arimilli resolves the appeal, we need not and do not consider Intel's arguments regarding this other ground.

reasonable mind might accept as adequate to support a conclusion." *Consol. Edison Co. v. N.L.R.B.*, 305 U.S. 197, 217 (1938).

B

In challenging the conclusion of nonobviousness over King and Arimilli, Intel argues that the Board committed legal error by requiring Intel to explain how the two relevant aspects of the two references could "bodily incorporated."

"The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference[.]" *Allied Erecting & Dismantling Co. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) (quoting *In re Keller*, 642 F.2d 413, 425 (C.C.P.A. 1981)). Instead, the question is whether "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention[.]" *Id.* (quoting *Pfizer, Inc. v. Apotex, Inc.,* 480 F.3d 1348, 1361 (Fed. Cir. 2007)); *see also In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) ("It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements."); *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (explaining that whether one reference can be incorporated in another is "basically irrelevant" since the test for obviousness is "not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole").

Intel argues that the Board required Intel to prove that Arimilli's caching mechanism, including its specific bus structure, could be "bodily incorporated" into King's bus system. That is clearly what happened here. The Board's only explanation for why claim 4 is nonobvious is that Intel had not shown a sufficient "rationale" for modifying King to accommodate Arimilli because "Intel has not specifically

explained **how** a [POSA] would have modified King[] . . . to **incorporate** a shared bus as disclosed in Arimilli." *Board Decision* at 38 (emphases added); *see also id.* (stating that the proposed combination requires "a modification that is not disclosed in King or Arimilli"). The Board did not find—and PACT does not argue—that Arimilli's L3 cache operating in shared mode does not teach the shared cache limitation of claim 4. To the contrary, the Board recognized that Arimilli teaches L3 caches and that latency of memory access can be improved "by operating the L3 caches in 'shared mode,' in which 'all L3 caches within the SMP data-processing system are combined, each L3 cache representing different segments of the system memory.'" *Board Decision* at 25 (citing Arimilli at 1:51–64, 4:64–66).

PACT disagrees that the Board required evidence of bodily incorporation and argues that the Board instead merely "rejected" that "King's [bus system] could be modified to include Arimilli's L3 caches[.]" Appellee's Br. at 36. But that is not the case. To be sure, evidence that the teachings and concepts of the prior art were (either actually or apparently) incompatible such that a skilled artisan would not have reasonably expected to succeed in combining those teachings is relevant to the obviousness analysis. But the Board never made a factual finding that King's bus system could not be modified to include Arimilli's L3 caches operating in shared mode. As we just explained, the Board merely stated that combining the relevant aspects of the two references requires a modification that the references did not teach and that Intel did not provide. *Board Decision* at 38.

In sum, the Board legally erred in requiring evidence that Arimilli's specific caching mechanism could be "bodily incorporated" into King's bus system. *See Elbrus Int'l Ltd. v. Samsung Elecs. Co.*, 738 F. App'x 694, 698 (Fed. Cir. 2018) (rejecting a similar argument that a proposed combination of references "would lead to an inoperable circuit

absent significant additional design work" as improperly requiring bodily incorporation to show obviousness).

C

Intel argues that, if we find that the Board legally erred by requiring evidence of bodily incorporation, then we should reverse because "[a]ll elements of claim 4 are admittedly disclosed[,] PACT made no arguments about secondary considerations[,] [a]nd PACT made no other arguments that the combination of King and Arimilli would be nonobvious." Appellant's Br. at 47. PACT does not address in its brief whether, if we agree with Intel that the board improperly required evidence of bodily incorporation, reversal is warranted. For the reasons below, we agree with Intel that reversal is warranted in this case.

Under a proper analysis, the Board should have asked whether an artisan of ordinary skill would have been motivated to combine the teachings of Arimilli and King to arrive at the claimed invention. Based on the evidence before the Board, we hold that substantial evidence could *only* support a finding that an ordinary artisan would have been so motivated. The '631 patent, Arimilli, and King are all concerned with improving the processing speed of multiprocessor systems. And King, while not using caching in its multiprocessor systems, *specifically* teaches that caching was an alternative method for improving processing speed. Taken altogether, there is strong evidence of motivation to combine. *See Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1341 (Fed. Cir. 2020) (reversing Board's finding that motivation was lacking where the two prior art references taught "two known, finite, predictable solutions for solving the same problem which, consistent with precedent, renders obvious the challenged limitation"); *In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1380 (Fed. Cir. 2007) ("One skilled in the art would naturally look to prior art addressing the same problem as the invention at hand, and in this case would find an appropriate solution."); *In re Kurzweil*,

4 F. App'x 823, 826 (Fed. Cir. 2001) ("The motivation to combine references can be inferred from the fact that they address the same problem."); *Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573 (Fed. Cir. 1996) ("[The motivation to combine references] may also come from the nature of the problem to be solved, leading inventors to look to the references relating to possible solutions to that problem."). Indeed, the Board found that an artisan of ordinary skill would have been motivated to combine Arimilli's lower-level caches when it found claims 2 and 3 obvious. *See Board Decision* at 30–33.

In its brief, PACT cites portions of its expert's declaration that it contends support the Board's conclusion that there was no motivation to combine the teachings of King and Arimilli. *See* Appellee's Br. at 37 (citing J.A. 3513–16 at ¶¶ 46–50). These paragraphs, however, do not change our conclusion that substantial evidence could only support a finding of motivation to combine. Some of the cited opinions, like the Board's flawed analysis, focus on whether the two references could be bodily incorporated without modification. *See* J.A. 3513–15 at ¶ 46 ("But [Arimilli's L3 caches operating in shared mode] is not possible in King's system, *without modification*." (emphasis added)), ¶ 48 ("King's bus units are not designed to transfer requests or data between processor buses and *neither King nor Arimilli teaches such a modification*. (emphasis added)), ¶ 50 ("[Intel's expert] *does not explain how POSITA would modify* King's bus units . . . ." (emphasis added)). Consequently, these opinions are "basically irrelevant." *In re Etter*, 756 F.2d at 859. Other opinions focus on Arimilli's L3 caches operating in "private" mode, rather than shared mode, *see* J.A. 3514–15 ¶¶ 47, 49, and are also irrelevant.

The only cited portion of the expert declaration relevant to the motivation inquiry is the opinion that

> At the very least, [modifying King's system to accommodate Arimilli's cache system] would require

> additional arbitration logic . . . . Such a modification would increase latency and contention for the processor buses, which goes directly against King's teachings that the system should "allow processors in a multi-processor system to access memories with a minimum of contention."

J.A. 3515–16 ¶ 50 (citing King at 1:46–50). PACT's expert does not opine how much the modification would increase latency or whether the latency introduced by the additional arbitration logic would be offset by the ability for the cache cores to operate as a single large cache. In other words, PACT's expert merely opines that there is an unspecified processing speed "cost" associated with implementing Arimilli's L3 caches in King's bus system but does not opine on whether the benefits of the implementation outweigh the cost. In light of the strong evidence of a motivation to combine set out above, this opinion and other evidence cited by PACT do not amount to substantial evidence that would support a conclusion of no motivation to combine.

III

For these reasons, we reverse the Board's determination that claim 4 of the '631 patent would not have been obvious.

REVERSED